

**INFORMATION DISCLOSURE CITATION**  
(Us several sh ets if n c ssary)

10996 U.S. PTO  
09/916509  
07/30/01

Atty. Docket No. 04329.2613	Serial No. Not Yet Assigned
Applicant Katsuhiko HIEDA	
Filing Date July 30, 2001	Group

**U.S. PATENT DOCUMENTS**

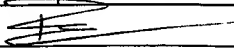
Examiner Initial*	Document Number	Date	Name	Class	Sub Class	Filing Date If Appropriate
TL	4,979,014	12/18/90	Hieda et al.			
TL	5,466,621	11/14/95	Hisamoto et al.			

**FOREIGN PATENT DOCUMENTS**

	Document Number	Date	Country	Class	Sub Class	Translation Yes or No
TL	6-9245	2/2/94	Japan			0Abstract
TL	2582794	11/21/96	Japan			Abstract

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

	Digh Hisamoto et al., "A FOLDED-CHANNEL MOSFET FOR DEEP-SUB-TENTH MICRON ERA" IEDM Technical Digest (Dec. 1998), pp1032-1034
	Digh Hisamoto et al., "A FULLY DEPLETED LEAN-CHANNEL TRANSISTOR (DELTA), - A novel vertical ultra thin SOI MOSFET -," IEDM Technical Digest (Dec. 1989), pp833-836
	K. Hieda, "NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES", IEDM 87, (Dec. 1987), pp 736-739

Examiner 	Date Considered 7 May 02
*Examiner: Initial if reference considered, whether or not citation is in conf ormance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	